

**CLAIMS**

1. A CAM cell with masking made in the form of an integrated circuit, including:  
a first storage cell arranged between two first bit lines, and including, in series, a first transistor, first and second inverters in anti-parallel, and a second transistor, gates of the first  
5 and second transistors being connected to a first word line;  
a comparison cell, including third and fourth transistors arranged between the first bit lines, a connection point of the third and fourth transistors controlling a fifth transistor, connected in series with a sixth inhibiting transistor between a result line and a bias voltage;  
a second storage cell, including, between second bit lines, a seventh transistor in series  
10 with two inverters in anti-parallel and an eighth transistor, the second storage cell controlling the inhibiting transistor;  
wherein the first, second, seventh, and eighth transistors are transistors having a channel of a first type, and the third, fourth, fifth, and sixth transistors are transistors with a channel of the opposite type.  
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2. The cell of claim 1, wherein the transistors having a channel of opposite type are P-channel transistors and are formed in a same N well.
3. The cell of claim 2, wherein the first, second, seventh, and eighth transistors, as  
20 well as the N-channel transistors of the inverters, are formed in a substantially aligned way and the P-channel transistors, as well as the P-channel transistors of the inverters, are formed in a substantially aligned way.